Training

PCI EXPRESS 3.1 ARCHITECTURE

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INTRODUCTION

The PCI Express System Architecture course starts with a high-level view of design to provide the big-picture context and then drills down into the details for each part of the design, providing a thorough understanding of the hardware and software protocols.

This course describes additional features added to the architecture when moving from PCIe specification revision 1.1 to 2.0 to 2.1 to 3.0 and 3.1. PCIe 3.0 (Gen 3) doubles the bandwidth available in revision 2.0 (Gen 2) by increasing the transfer rate and dropping 8b/10b encoding. A number of protocol changes were also implemented in the change from revision 2.0 to 2.1. The changes in Gen 3 are related to physical layer updates that will support the higher speed, including some new steps for link training to get the speed working reliably. All these changes will be further elaborated during the training.

TARGET AUDIENCE

This course is hardware-oriented but is suitable for both hardware and software engineers. This course is ideal for RTL Design Engineers, Chip Design Engineers, System Design Engineers, or System Board-Level Design Engineers who need a broad understanding of PCI Express. This course is also suitable for chip-level and board-level Validation Engineers.

RECOMMENDED PREREQUISITES

A basic understanding of digital bus architectures such as PCI is highly recommended.

KEY LEARNING POINTS

In this course, participants will learn more about:

- PCI Express features, capabilities, and the definition of each layer of interface
- How hardware-based automatic error detection and correction mechanism work
- Packet-based protocol used by PCIe
- Address space and packet-routing methods
- Power management techniques
- Configuration register details that provide control and status visibility to software
- ECNs related to PCI Express 2.1 and 3.1 specification and the changes needed to run the link at 8.0 GT/s (Rev 3.0 Speeds)

TRAINING OUTLINE

1. PCI Architecture Background Foundation
   - PCI Legacy Configuration Transaction Generation
2. PCI Express Features and Architecture Overview
   - Layered Architecture
   - TLP, DLLP, and Ordered Set Packet Format Overview
   - Protocol Overview
3. Configuration Overview
   - Legacy and Enhance Configuration Transaction Generation
   - Header 0/1, Capability, and Extended Capability Register Overview
   - Bus Enumeration
   - Arbor Lab: Scan Your System and Determine Topology
4. Address Space and Transaction Routing
   - Switch Routing Mechanism
   - Arbor Lab: Debug Problem with Plug-and-Play Address Mapping
5. TLP Format Details
6. Quality of Service and Arbitration
   - TC/VC Mapping and VC/Port Arbitration
7. Flow Control
   - Flow Control Initialization
   - Runtime Flow Control Update Mechanism
8. Transaction Ordering
   - Simplified Ordering Table (2.1)
   - ID-Based Ordering (2.1)
9. DLLP Format Details
10. ACK/NAK Protocol
    - Error Recovery Mechanism
    - Examples of Variety of Error Scenarios
    - Nullified Packets and Store-and Forward vs Cut-Through Mode
11. Physical Layer Logic (Gen1/Gen2)
    - Byte Striping/Unstriping
    - Scrambling/Unscambling
    - 8b/10b Encoding/Decoding
    - Serializing/Deserializing

TRAINING OUTLINE *(cont)*

12. Physical Layer Logic (Gen3)

- 128b/130b Encoding/Decoding

13. Physical Layer Electrical (Gen1/Gen2/Gen3)

- Differences Between Generations
- De-Emphasis
- Gen3 Equalization

14. Link Initialization and Link Training

- Detect, Polling, Configuration, L0, Recovery (Retraining) States
- Power Management States: L0, L0s, L1, L1 Active, L2, L3 Power States
- Gen3 Equalization Training
- Link Width and Speed Changing

15. Error Detection and Handling

- Correctable, Non-Fatal and Fatal Errors
- Arbor Lab: Determine Source and Error Reporting Mechanism

16. Power Management

- Software-Controlled Power Management
- Active Hardware-based Power Management
- Optimized Buffer Flush Fill (OBFF) (2.1), Latency Tolerance Reporting (2.1), and L1 Sub-States (3.1)

17. Interrupt Support

- Legacy Interrupt Handling
- MSI Interrupt
- MSI-X Interrupt
- Arbor Lab: Investigate Source of MSI Interrupt and Delivery

18. System Resets

- Fundamental Reset (Cold and Warm Reset) and In-band Reset (Hot Reset)
- Function Level Reset (FLR)

19. Hot Plug and Power Budgeting

- Hot Plug Controller
- Dynamic Power Allocation (2.1)

TRAINING OUTLINE *(cont)*

20. 2.1 and 3.1 ECN

- **Internal Error Reporting**
- **Multi-Casting**
- **Atomic Operations**
- **Resizable BARs**
- **Alternative Routing-ID Interpretation**
- **Extended Tag Enable**
- **TLP Processing Hints**
- **Downstream Port Containment**
- **Lightweight Notification**
- **Process Address Space ID**
- **Precision Time Measurement**
- **Protocol Multiplexing**
- **Address Translation Services**

DURATION

5 Days (9.00 am – 5.00 pm)

TRAINING DATE(S) & VENUE

25 – 29 September 2017 @ PSDC, Penang

COURSE FEE

RM7,250/participant (excluding 6% GST). Course fees are HRDF claimable.

TRAINING MATERIALS

- PCI Express Technology eBook (covers PCIe 3.0)
- Downloadable PDF version of the Presentation Slides

TRAINER'S PROFILE

RAVI BUDRUK

Vice President – Mindshare, Inc

Mr Ravi Budruk is Vice President at MindShare, a technology training company. He has over 20 years of industry experience.

Prior to joining MindShare, Mr Budruk was an Intel processor-based Chipset Design Engineer, System Architect, and Manager at VLSI Technology, Inc. Mr Budruk has trained thousands of hardware and software engineers in various subjects of computer architecture. Mr Budruk is an industry expert on topics such as Intel x86 Processor Architecture, bus architectures such as Intel QuickPath Interconnect, HyperTransport, PCI Express.PCI/PCI-X, IEEE 1394, ISA, PC System architecture, and a variety of memory (DDRx) technologies. He is an excellent presenter and a dynamic speaker who brings industry-acquired experience to the class.

Mr Budruk has a Master's of Science degree in Electrical Engineering from Purdue University and a Bachelor of Science degree (*Magna cum Laude*) in Electrical Engineering from Texas Tech University. Ravi Budruk is also the author of the 'PCI Express System Architecture' textbook. As Vice President at MindShare, he manages the business.

ADMINISTRATIVE DETAILS

Cancellation Policy:
The PSDC reserves the right to cancel or postpone the program but with due notice to the participating company. For any cancellation or postponement of training by the participating company, a written notification by email must be sent to the PSDC. Cancellation/postponement charges are calculated based on the following:

Receipt of Cancellation/Postponement Notification	***Charges/Penalty***
Seven (7) working days prior to the commencement of training	*Nil*
Less than seven (7) working days prior to the commencement of training	*50% of package fee*
On the day of the training	*Full package fee*

Online Registration:
To register, log on to http://www.psdc.org.my or contact our sales personnel below.

Enquiries:
For further information, please contact: Elly Leong (ext 523/ellyleong@psdc.org.my)
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To find out more, call our **Corporate Training Team ext 523/577/514/517/596** or email to **corptraining@psdc.org.my**

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